AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An article comprising a machine-accessible medium having stored thereon instructions that, when executed by a machine, cause the machine to:

obtain from a performance monitor runtime performance data of a thread level utilization of the machine by an application during an execution of the application on the machine, wherein the runtime performance data is indicative of a set of execution characteristics of a thread of the application, including an instructions-per-clock cycle metric and a memory references-per-clock cycle metric, wherein the runtime performance data includes instruction counts, memory references, and cycle counts obtained from a timer interrupt in the performance monitor; and

based on the instructions-per-clock cycle metric and the memory references-per-clock cycle metric, reduce power dissipation of the machine by adjusting an operating voltage or an operating frequency of the machine during the execution of the application, wherein the operating voltage and operating frequency are nonzero.

2. (Previously Presented) The article of claim 1, wherein the performance monitor is a Performance Monitoring Unit (PMU) and is part of a central processing unit (CPU) within the machine.

3. (Canceled)

4. (Previously Presented) The article of claim 5, wherein the PMU includes a plurality of counters for simultaneously measuring multiple different performance data.

5. (Previously Presented) The article of claim 2, wherein the runtime performance data includes at least one from the group consisting of instruction cache misses, data cache misses, instructions executed, branches executed, branch mis-predicts, instruction translation look-up buffer TLB misses, data translation look-up buffer TLB misses, stalls due to data dependency, and data cache write-backs.

6. (Previously Presented) The article of claim 1, having further instructions that, when executed by the machine, cause the machine to:

in response to the runtime performance data, determine if the operating voltage and operating frequency should be adjusted upward or scaled down.

7. (Previously Presented) The article of claim 6, having further instructions that, when executed by the machine, cause the machine to:

compare the runtime performance data to a voltage and frequency scheduler lookup table that stores at least one voltage value and at least one frequency value.

8. (Currently Amended) The article of claim 1, having further instructions that, when executed by the machine, cause the machine to:

simultaneously obtain a plurality of runtime performance data; and

in response to the plurality of runtime performance data, ~~adjusting~~ adjust the operating voltage and the operating frequency.

9. (Canceled)

10. (Canceled)

11. (Original) The article of claim 1, having further instructions that, when executed by the machine, cause the machine to:

operate the performance monitor in an operating system environment in communication with a platform hardware environment, in a kernel mode, and in communication with an end user code, in a user mode.

12. (Original) The article of claim 1, wherein the instructions, when executed by the machine, cause the machine to adjust the operating voltage and the operating frequency.

13. (Previously Presented) A method comprising:

obtaining, from a performance monitor, runtime performance data of a thread level utilization of a machine by an application during an execution of the application on the machine, wherein the runtime performance data is indicative of a set of execution characteristics of a thread of the application, including an instructions-per-clock cycle metric and a memory references-per-clock cycle metric for a central processing unit (CPU) having an operating voltage and an operating frequency; and

reducing power dissipation of the CPU by adjusting the operating voltage or the operating frequency during the execution of the application in response to the instructions-per-clock cycle metric and the memory references-per-clock cycle metric, wherein the operating voltage and operating frequency are nonzero.

14. (Original) The method of claim 13, further comprising:
adjusting both the operating voltage and the operating frequency.

15. (Original) The method of claim 14, further comprising adjusting the operating voltage and the operating frequency upward.

16. (Original) The method of claim 14, further comprising adjusting the operating voltage and the operating frequency downward.

17. (Original) The method of claim 13, wherein the performance monitor is a Performance Monitoring Unit (PMU).

18. (Previously Presented) The method of claim 13, wherein the runtime performance data includes at least one from the group consisting of instruction cache misses, data cache misses, instructions executed, branches executed, branch mis-predicts, instruction translation look-up buffer misses, data translation look-up buffer misses, stalls due to data dependency, and data cache write-backs.

19. (Currently Amended) The method of claim 13, further comprising comparing the runtime performance data to a voltage and frequency scheduler lookup table that includes at least one voltage value and at least one frequency value.

20. (Original) The method of claim 19, further comprising:

benchmarking the CPU;

determining the at least one voltage value and the at least one frequency value in response to the benchmarking; and

creating a lookup table of the at least one voltage value and the at least one frequency value.

21. (Canceled)

22. (Previously Presented) A method for adjusting operating voltage and/or operating frequency on a machine having a processor, the method comprising:

the machine simultaneously monitoring multiple performance events, where each performance event reflects a different thread level utilization of the processor by at least one application during an execution of the at least one application on the processor;

based on the simultaneously monitored multiple performance events, obtaining multiple performance metrics indicating events per clock cycle of a thread of the at least one application; and

based on the multiple performance metrics, reducing power dissipation of the machine by adjusting an operating voltage or an operating frequency of the machine during the execution of the at least one application.

23. (Previously Presented) The method of claim 22, wherein the multiple performance metrics include an instructions-per-clock cycle metric and a memory references-per-clock cycle metric.

24. (Previously Presented) The method of claim 22, wherein the performance events are instruction counts and memory references that are simultaneously monitored.

25. (Previously Presented) The method of claim 22, further comprising the machine simultaneously monitoring multiple performance events from different applications executing on the processor.

26. (Previously Presented) The method of claim 22, further comprising simultaneously monitoring the multiple performance events using a different counter dedicated to monitor for each performance event.